Shape and nature of killer defects in 3C-SiC as revealed by molecular dynamics simulation of stacking fault evolution

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Using atomistic simulations we address a key issue in the SiC technology, namely the origin of ubiquitous defects, which degrade the electronic characteristics of 3C-SiC epitaxial layers on Si(001) substrates. We provide a detailed understanding of the mechanism at the base of the stacking fault evolution during 3C-SiC layer growth, also providing an explanation for the abundance of twinned region, formed by three successive stacking faults and finally, we reveal their impact on the electronic properties of the crystal.

First, the evolution of a single partial dislocation loop releasing tensile strain has been analyzed by MD simulations. We found that this evolution ends with the formation of the experimentally observed V- or Δ-shaped stacking fault planes [1] (see Fig. 1a). We also demonstrate that the different mobility of the diverse partial dislocation segments, composing the dislocation loop terminating the SF, plays a key role [2]. Thereafter, we show that the nucleation of new loops in the vicinity of the first one may lead to the formation of multiple stacking faults, efficiently decreasing the elastic energy of the crystal. Our findings agree with the experimental evidence that the occurrence of multiple SFs increases when thick 3C-SiC films on Si(001) substrate are grown[3]. In particular, the excess free energy is minimized via the formation of a triple stacking fault with a common boundary made up of dislocation complexes and yielding a null total Burgers vector, as shown in Fig. 1b.

The atomic structures of dislocation complexes formed at the boundary of multiple stacking faults have been then used as input for DFT calculations, which are typically more accurate and thus are suited for refining the atomic structure of the dislocation core and to investigate their electronic properties (see Fig. 2). It turns out that the partial dislocation complexes terminating double and triple SFs are responsible for the introduction of electronic states significantly filling the band gap [4] and likely causing degradation of the device performance, particularly in terms of leakage current.

Understanding how 3C-SiC growth conditions influence the stacking faults is crucial to find new methods for reducing multiple stacking fault concentration. Our study impacts both experimental and theoretical studies on 3C-Si, contributing to the advances in the 3C-SiC technology for power devices.

Fig. 1. **a)** Snapshots of two molecular dynamics simulations of stacking fault evolution in 3C-SiC. The final structure of the defect is Δ-shaped on (111) and (11̅1) planes while is V-shaped on (1̅1̅1) and (1̅1̅1̅) planes. **b)** Elastic energy of multiple loop complexes, in the first column loops boundaries are separated, in the second column loop boundaries are closer and in the third column loop boundaries join. First row – two adjacent loops with same Burgers vector; second row – two adjacent loops with different Burgers vector; third row – three adjacent loop with three different Burgers vector. The elastic energy decreases when loops with different Burgers vectors form a common boundary.

Fig. 2. Defect states at the triple dislocation complex boundary: On the left a triple stacking fault and its boundary; on the right the Kohn-Sham eigenvalue spectra of one of the dislocation cores is plotted, with the blue (red) lines indicating occupied (unoccupied) states and the two dashed lines indicating VB and CB edges in the pristine SiC. The side views of the dislocation core with the charge densities of the corresponding gap states are also illustrated.